Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of forming a metal oxide semiconductor effect transistor (MOSFET) on a semiconductor substrate, comprising the steps of:

forming a gate insulator layer on said semiconductor substrate;

performing a procedure to form a nitrided gate insulator layer;

performing ~~an~~ a hydrogen anneal procedure;

forming a conductive gate structure on a portion of said nitrided gate insulator layer;

forming a lightly doped source/drain region in an area of said semiconductor substrate not covered by said conductive gate structure;

forming insulator spacers on sides of said conductive gate structure; and

forming a heavily doped source/drain region in an area of said semiconductor substrate not covered by said conductive gate structure or by said insulator spacers.

2. (Original) The method of claim 1, wherein said gate insulator layer is a silicon dioxide layer, obtained via a thermal oxidation procedure at a thickness between about 10 to 30 Angstroms.

3. (Original) The method of claim 1, wherein said nitrided gate insulator layer is a nitrided silicon dioxide layer, at an equivalent oxide thickness between about 7 to 20 Angstroms.

4. (Original) The method of claim 1, wherein said nitrided gate insulator layer is comprised with a dielectric constant between about 3.9 to 7.8.

5. (Original) The method of claim 1, wherein said procedure used to form said nitrided gate insulator layer is a plasma nitridation procedure, performed at a power between about 10 to 5000 watts, for a time that is sufficient to obtain a desired nitrogen content in a top portion of said gate insulator layer, with the plasma nitridation procedure performed in ambient comprised of N_2 and helium, or of N_2 and argon.

6. (Original) The method of claim 1, wherein said procedure used to form said nitrided gate insulator layer is an anneal procedure performed at a temperature between about 600 to 1100°C, for a time sufficient to obtain a desired nitrogen constant in said gate insulator layer, performed in ambient comprised of either NH_3, NO, or N_2O.

7. (Currently Amended) The method of claim 1, wherein said hydrogen anneal procedure is performed to said nitrided gate insulator layer in a single wafer rapid thermal annealing (RTP), or in a batch type furnace system, performed in a hydrogen ambient at a temperature between about 800 to 1100°C, for a time between about 0.5 to 10 min.

8. (Currently Amended) The method of claim 1, wherein said hydrogen anneal procedure is performed in situ, in the same tool to be used for deposition of a conductive gate material, with the anneal performed at a temperature between about 600 to 800°C, for a time between about 30 to 150 sec., using a hydrogen/nitrogen ratio that features a hydrogen percentage between about 10-50.

9. (Original) A method of forming a MOSFET device on a semiconductor substrate comprising the steps of:

forming a silicon dioxide insulator layer on said semiconductor substrate;

performing a procedure to form a nitrided silicon dioxide layer;

performing a hydrogen anneal proceure;

forming a polysilicon gate structure on said hydrogen annealed nitrided silicon dioxide layer;

forming a lightly doped source/drain region in an area of said semiconductor substrate not covered by said polysilicon gate structure;

forming insulator spacers on sides of said polysilicon gate structure;

forming a heavily doped source/drain region in an area of said semiconductor substrate not covered by said polysilicon gate structure or by said insulator spacers.

10. (Original) The method of claim 9, wherein said silicon dioxide later is obtained via a thermal oxidation procedure, to a thickness between about 10 to 30 Angstroms.

11. (Original) The method of claim 9, wherein said procedure used to form said nitrided silicon dioxide layer is a plasma nitridation procedure, performed at a power between about 10 to 5000 watts, for a time that is sufficient to obtain a desired nitrogen content in a top portion of said silicon dioxide gate insulator layer, with the plasma nitridation procedure performed in ambient comprised on N_2 and helium, or comprised of N_2 and argon.

12. (Original) The method of claim 9, wherein said procedure used to form said nitrided silicon dioxide layer is an anneal procedure performed at a temperature between about 600 to 1100°C, for a time sufficient to obtain a desired nitrogen content in said silicon dioxide gate

insulator layer, wherein said anneal procedure is performed in ambient comprised of either NH_3, NO, or N_2O.

13. (Original) The method of claim 9, wherein said nitrided silicon dioxide layer is comprised with an equivalent oxide thickness between about 7 to 20 Angstroms.

14. (Original) The method of claim 9, wherein said nitrided silicon dioxide layer is comprised with a dielectric constant between about 3.9 to 7.8.

15. (Original) The method of claim 9, wherein said hydrogen anneal procedure is performed in a single wafer rapid thermal annealing (RTP), or in a batch type furnace system, performed in a hydrogen ambient at a temperature between about 800 to 1100°C, for a time between about 0.5 to 10 min.

16. (Original) The method of claim 9, wherein said hydrogen anneal procedure is performed in situ with the same tool to be used for deposition of a polysilicon gate material, with said hydrogen anneal procedure performed at a temperature between about 600 to 800°C, for a time between about 30 to 150 sec., using a hydrogen/nitrogen ratio that features a hydrogen percentage between about 10-50.

17. (Currently Amended) A method of forming a metal oxide semiconductor field effect transistor (MOSFET) on a semiconductor substrate, comprising the steps of:

forming a silicon dioxide gate insulator layer on said semiconductor substrate;

performing ~~an~~ a hydrogen anneal procedure;

forming a polysilicon gate structure on a portion of said silicon dioxide gate insulator layer;

forming a lightly doped source/drain region in an area of said semiconductor substrate not covered by said polysilicon gate structure;

forming insulator spacers on sides of said polysilicon gate structure; and

forming a heavily doped source/drain region in an area of said semiconductor substrate not covered by said polysilicon gate structure or by said insulator spacers.

18. (Original) The method of claim 17, wherein said silicon dioxide gate insulator layer is obtained via a thermal oxidation procedure at a thickness between about 10 to 30 Angstroms.

19. (Currently Amended) The method of claim 17, wherein said hydrogen anneal procedure is performed in a single wafer rapid thermal annealing (RTP), or in a batch type furnace system, performed in a hydrogen ambient at a temperature between about 800 to 1100°C, for a time between about 0.5 to 10 min.

20. (Currently Amended) The method of claim 17, wherein said hydrogen anneal procedure is performed in situ, in the same tool to be used for deposition of a polysilicon gate material, with the anneal performed at a temperature between about 600 to 800°C, for a time between about 30 to 150 sec., using a hydrogen/nitrogen that features a hydrogen percentage between about 10-50.